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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,847	10/03/2003	Peter T. Sleeman	DYOUP0258US	2425

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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 10/678,847	**Applicant(s)** SLEEMAN, PETER T.	
	Examiner Tanh Q. Nguyen	**Art Unit** 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-8, 11, 14, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by TEXAS INSTRUMENTS, INC.; TL16PC564B, TL16PC564BLV PCMCIA Universal Asynchronous Receiver Transmitter; SLLS225A (hereinafter TI).

3. As per claim 1, TI teaches an interface device [PCMCIA UART, p.3] for enabling communications between a host and a subsystem, comprising:

a register set comprising a plurality of registers configurable to control host-subsystem communications according to a UART standard [registers on pp. 7-8];

a host interface configurable to establish data communication with the host [Host CPU/UART interface, p. 10];

a serial interface [subsystem/UART interface, p. 10; UART TL16C550C, p. 3] configurable to establish a bi-directional serial data communication channel to the subsystem [SIN, SOUT, p. 6] under the control of the register set [registers on pp. 7-8]; and

a parallel interface configurable to establish an auxiliary parallel data communication channel to the subsystem operable in conjunction with the serial data communication channel [subsystem serial-bypass mode allows direct parallel access to the receiver FIFO and the transmitter FIFO, p. 12 - hence a parallel interface for auxiliary parallel communication channel with the subsystem], wherein the parallel interface operates under control of the register set [registers on pp. 7-8].

4. As per claims 3-8, TI further teaches supplementary FIFO data buffers [expanded 6x11 receiver FIFO and 64x8 transmitter FIFO, p. 1] for writing and reading data to and from the subsystem via the parallel interface, wherein one of the registers is mapped to at least one of the supplementary data buffers so that accesses to the mapped register will cause accesses to the at least one of the supplementary data buffers [UART transmitter FIFO (read only) and UART receiver FIFO (write only) when serial-bypass mode is enabled, p. 8 and p. 12];

5. As per claims 11, 14, TI teaches the UART standard being the 16550 standard [UART TL16C550C, p. 3];

the interface device for connecting a host and a subsystem [p. 1 and p. 3] - hence a system comprising a host, a subsystem and the interface.

6. As per claim 17, TI teaches a method of communicating data between a host and a subsystem, comprising:

establishing a bi-directional serial data communication link [SIN, SOUT, p. 3] with the subsystem under control of a register set conforming to a UART standard [registers on pp. 7-8];

establishing an auxiliary parallel data communication link with the subsystem [subsystem serial-bypass mode allows direct parallel access to the receiver FIFO and the transmitter FIFO, p. 12] also under control of the register set [registers on pp. 7-8];

and

transferring data over the auxiliary parallel data communication link to bypass the serial data communication link [subsystem serial-bypass mode allows direct parallel access to the receiver FIFO and the transmitter FIFO, p. 12].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9-10, 12-13, 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over TI.

9. As per claims 9-10, TI teaches the claimed invention except for - first control and status lines connected between each data buffer and the register set, and second control and status lines connected between each data buffer and the parallel interface.

Since it was known in the art at the time the invention was made to use control and status lines between a data buffer and a source, and between the data buffer and a destination in order to control read from and write to the data buffer, indicate data level in the data buffer, and ensure proper operation of the data buffer, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include control and status lines connected between each data buffer and the register set to communicate control and status signals to and from each buffer from the host side, and to include control and status lines connected between each data buffer and the parallel interface to communicate control and status signals to and from each buffer from the subsystem side - in order to control read from and write to the data buffers, indicate data level in the data buffers, and ensure proper operation of the data buffers.

10. As per claims 12-13, TI teaches the claimed invention except for a card comprising the interface integrated with a subsystem, and except for the subsystem including a wireless interface for communicating with a third party data transceiver.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate a subsystem with the PCMCIA UART on a card, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. Howard v. Detroit Stove Works, 150 U.S. 164 (1893).

Furthermore, TI teaches the subsystem being a modem [p. 1]. Since it was known in the art at the time the invention was made for a wireless modem to include a wireless interface in order to communicate wirelessly with a third party data transceiver, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a wireless interface - in order to communicate wirelessly with a third party data transceiver.

11. As per claims 15-16, TI teaches the claimed invention except for the serial communication data channel and the auxiliary parallel communication data channel including wireless portions, or being made exclusively of fixed links.

Since it was known in the art at the time the invention was made to include wireless portions in data communication channels to allow for wireless communications, or to include fixed links in data communications to allow for wired communications, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the serial and auxiliary parallel communication data channels to include wireless portions - in order to communicate wirelessly, or to include fixed links - in order to enable wired communication.

Response to Arguments

12. Applicant's arguments filed April 27, 2006 have been fully considered but they are not persuasive.

13. Applicant argued that - TI discloses a device in which control of host-subsystem communications requires an additional register that is not part of the UART standard. This additional register is the Subsystem Control Register (see page 11). This non-standard register is required to activate the serial-bypass mode (see last paragraph in section headed "Subsystem Control Register" on page 11). Thus, TI does not disclose a register set that is "configurable to control host-subsystem communications according to a UART standard", as recited in feature (a) of claim 1.

Applicant's argument is not persuasive because the claim merely recites "a register set comprising a plurality of registers configurable to control host-subsystem communications according to a UART standard". Since TI discloses a register set comprising UART registers and host-subsystem communications being in accordance with a UART standard (see rejections above), TI teaches the limitation of the claims. The limitation does not preclude a register set being comprised of UART registers and an additional (non-standard) subsystem control register.

14. Applicant also argued that - in TI the serial-bypass mode (as its name suggests) simply bypasses the serial communications link when increased data throughput is required. At times when the serial-bypass mode is enabled, the serial communication channel is disabled and cannot be used. This is because both channels rely on the same internal FIFO buffers, e.g., see under the heading "subsystem serial-bypass mode on page 12. Accordingly, TI also does not teach an interface device having "an auxiliary parallel data communication to the subsystem operable in conjunction with the serial data communication channel", as recited in claim 1. In TI the parallel channel can only be used as an alternative to the serial channel. TI does not allow both the serial and parallel channels to be used simultaneously.

Applicant's argument is not persuasive because the features upon which applicant relies (i.e., allowing both the serial and parallel channels to be used simultaneously) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Note that the limitation "an auxiliary parallel data communication to the subsystem operable in conjunction with the serial data communication channel" can reasonable be interpreted as "an auxiliary parallel data communication to the subsystem operable together with the serial data communication channel", and are therefore disclosed by TI (see the rejections above). The above limitation does not have the same meaning as "allowing both the serial and parallel channels to be used simultaneously".

15. Applicant further argued that - according to claim 1, the parallel interface of the present invention operates under control of the register set (see last line of claim 1). In TI, the serial-bypass mode does not operate under control of the register set. To the contrary, the serial-bypass mode operates by giving the subsystem direct parallel access to the internal UART read and transmit FIFOs (see under the heading "subsystem serial-bypass mode on page 12). That is to say the serial-bypass mode bypasses the registers and does not operate under control of them.

Applicant is not persuasive because the parallel interface operates under the control of the subsystem control register, which is comprised in the register set of TI (see rejections above).

16. Applicant last argued that - all of the above differences enable interface devices according to the claimed invention to be fully backward compatible with legacy architecture and software code, whereas the interface device of TI is not. The interface device of TI requires specially written software drivers to be implemented.

Applicant's argument is not persuasive because the features upon which applicant relies (i.e., to be fully backward compatible with legacy architecture and software code) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

17. Applicant's above arguments are also not persuasive because applicant did not

indicate where the support for applicant's arguments can be found in applicant's disclosure.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 30, 2006

TQN
June 30, 2006